REMARKS

Claims 40-58 are pending in the application with claims 40, 48, and 56 amended herein.

Claims 40-55 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Lur in view of Choe. Applicant requests reconsideration.

Amended claim 40 sets forth integrated circuitry that includes, among other features, an electrically insulating layer over a semiconductive substrate, a series of alternating first and second conductive lines spaced and positioned laterally adjacent one another directly over the insulating layer, and intervening insulating spacers laterally between the first and second conductive lines. The first conductive lines and the second conductive lines have respective line tops and the spacers have respective spacer tops that are substantially coplanar with at least some of the first and second conductive line tops. The first conductive lines are electrically isolated from the second conductive lines. The series of first conductive lines or the series of second conductive lines provide cross-talk shielding for the other series. Pages 2-3 of the Office Action allege that Lur discloses every limitation of claim 40 except for insulating spacers and relies upon Choe to remedy the deficiency. Applicant asserts that Lur in view of Choe fails to disclose or suggest every limitation of amended claim 40.

Page 2 of the Office Action alleges that polysilicon conductors 24 in Lur disclose the claimed series of alternating first and second conductive lines. Page 7 of the Office Action states any line in Lur can be labeled as a first conductive line or a second conductive line. However, Applicant notes that

the express terms of claim 40 set forth limitations upon the structural features and relative positions of lines that qualify as first or second conductive lines. For example, claim 40 sets forth that the first and second conductive lines are spaced and positioned laterally adjacent one another.

Consistent with Figs. 6 and 10 and elsewhere throughout the present specification, Applicant previously asserted that those of ordinary skill recognize "adjacent" to mean close to, lying near, next to, or adjoining. The Office Action fails to acknowledge or give weight to such express term of claim 40. Contrary to the requirements of 37 CFR 1.104(c)(2), the pertinence of Lur in showing laterally adjacent structures is not clearly explained since, on its face, those of ordinary skill would not consider Fig. 11 of Lur to show laterally adjacent structures. Figs. 6 and 10 of the present specification provide non-limiting examples of laterally adjacent structures in stark contrast to Fig. 11 of Lur. By comparison, polysilicon conductors 24 are not close to, do not lie near, are not next to, and do not adjoin one another. The Office Action merely draws the conclusion without clearly explaining why Lur nevertheless discloses laterally adjacent structures when the distances between structures are so different from the non-limiting examples in the present specification. Application requests clarification with detailed analysis of the express claim terms or withdrawal of the Office's relied upon reasoning.

Page 7 of the Office Action merely states that the present specification does not teach that distance between the conductors is of any significance in providing cross-talk shielding. To the contrary, the present specification

expressly states that the first and second conductive lines are laterally adjacent one another specifically to provide cross-talk shielding on page 6, lines 3-8, page 7, lines 24 to page 8, line 5, and elsewhere. Page 2, lines 16-20 of the present specification also discuss a prior art cross-talk shielding technique. In addition to the express disclosure in the present specification, those of ordinary skill recognize the well known importance of distance between a conductive line and its intended shield simply based upon principles of physics.

The Office Action attempts to allege that the present specification does not teach distance between conductors is significant in providing cross-talk shielding and ignores the significance of the claimed first and second conductive lines being laterally adjacent. Applicant previously asserted and herein reasserts that the relatively large distance between polysilicon conductors 24 in Lur precludes such conductors from being considered "laterally adjacent." Such is especially true in the context of providing cross-talk shielding. The Office Action fails to provide any evidence or technical reasoning in support of its finding that polysilicon conductors are laterally adjacent. Applicant asserts that those of ordinary skill, considering the claim 40 limitation that the claimed conductive lines provide cross-talk shielding and the asserted definition for "laterally adjacent," would clearly determine that polysilicon conductors 24 in Lur are not laterally adjacent. Accordingly, Lur fails to disclose every limitation of claim 40.

Also, Applicant notes that amended claim 40 sets forth that the series of alternating first and second conductive lines are directly over the insulating

layer over the semiconductive substrate. Even though page 2 of the Office Action alleges that polysilicon conductors 24 disclose both the first and second conductive lines, page 4 of the Office Action alters such allegation and states that polysilicon conductors 24 disclose the first conductive lines and electrode metal layers 40 discloses the second conductive lines. Page 2 of the Office Action alleges that gate dielectric 23 or field oxide isolation region 22 discloses the claimed electrically insulating layer. However, Applicant notes that Fig. 11, relied upon in the Office Action, shows an electrode metal layer 40 in a position that is not directly over either gate dielectric 23 or field oxide isolation region 22. Accordingly, Lur fails to disclose every limitation of amended claim 40.

Further, amended claim 40 sets forth that the first conductive lines are electrically isolated from the second conductive lines. However, Fig. 11 of Lur shows first electrode metal layer 40 electrically connected through contact stud 26 to polysilicon conductor 24. The claimed isolation structure provides the advantage of cross-talk shielding, as mentioned above. Lur does not contemplate any advantage to electrically isolating first electrode metal layer 40 from polysilicon conductor 24. Instead, Lur requires electrical contact of such structures through contact stud 26. Accordingly, Lur fails to disclose every limitation of claim 40.

Even if polysilicon conductors 24 are alleged to disclose the claimed first and second conductive lines, Applicant still asserts that such structures of Lur are not electrically isolated as set forth in claim 40. Column 4, lines 6-14 and elsewhere throughout Lur state that polysilicon conductors 24 are a

part of a very large scale integrated circuit. Polysilicon conductors 24 form the gates of transistors including source/drain regions 28 and gate dielectric 23. Those of ordinary skill readily recognize that the transistor gates of an integrated circuit such as shown in Fig. 11 of Lur cannot be electrically isolated, as set forth in claim 40, and still function as intended. Simply by forming part of an integrated circuit, polysilicon conductors 24 are necessarily electrically connected. Accordingly, Applicant asserts that Lur fails to disclose every limitation of claim 40.

Still further, page 2 of the Office Action alleges, without indicating any support in Lur, that such reference discloses providing cross-talk shielding. Page 3 of the Office Action addresses the lack of support in Lur by merely stating that such features are inherent in Lur since the claimed structure is identical to the structures described in Lur. Such an allegation ignores the requirement under 35 U.S.C. 103(a) that "the subject matter as a whole" must have been obvious at the time the invention was made. The Office must consider claim 40 as a whole. Notably, claim 40 is expressly written to encompass only integrated circuitry with a structure sufficient to provide cross-talk shielding. Arguably, without such a limitation, the remaining structural features of claim 40 encompass integrated circuitry that does not necessarily provide such cross-talk shielding. The Office Action admits that Lur fails to disclose cross-talk shielding and yet asserts the Lur structure is identical to the claim 40 structure that includes cross-talk shielding. Such an allegation fails the requirement of 35 U.S.C. 103(a) to consider the subject matter of claim 40 as a whole.

Understandably, it is possible to show that claim features are inherently disclosed. However, "the mere fact that a certain thing may result from a given set of circumstances is not sufficient to establish inherency." In re Rijckaert, 9 F.3d 1531, 1534, 28 USPQ2d 1955, 1957 (Fed. Cir. 1993) (citations omitted) (emphasis in original); MPEP 2112. Further, "[i]n relying upon the theory of inherency, the Examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art." Ex parte Levy, 17 USPQ2d 1461, 1464 (Bd. Pat. App. & Inter. 1990) (emphasis added); MPEP 2112. The Office Action fails to provide a sufficient basis in fact and/or technical reasoning sufficient to establish that Lur inherently discloses the cross-talk shielding of claim 40. The Lur structures do not necessarily provide cross-talk shielding.

As established above, Lur fails to disclose a series of alternating first and second conductive lines spaced and positioned laterally adjacent one another. Lur fails to disclose that the lines are directly over the electrically insulating layer. Lur fails to disclose that the first conductive lines are electrically isolated from the second conductive lines. Lur fails to disclose that the first or second conductive lines provide cross-talk shielding. Applicant further asserts that Lur fails to suggest any of the indicated claim limitations. The Office Action relies upon Lur in combination with Choe, however, Choe fails to disclose or suggest and the Office Action fails to allege that Choe discloses or suggests the subject matter of claim 40 absent from Lur. At least for such reason, claim 40 is patentable over Lur in view of Choe.

Claims 41-47 depend from claim 40 and are patentable at least for such reason as well as for the additional limitations of such claims not disclosed or suggested. For example, claim 42 sets forth that the first conductive lines' lateral cross-sectional shape is different from the second conductive lines' lateral cross-sectional shape. In the case that the Office Action alleges polysilicon conductors 24 disclose the first and second conductive lines, Lur fails to disclose the different cross-sectional shape set forth in claim 42. In the case that the Office Action alleges that polysilicon conductors 24 disclose the first conductive lines and electrode metal layers 40 disclose the second conductive lines, Lur fails to disclose the limitation that the first conductive lines are electrically isolated from the second conductive lines. At least for such reason, claim 42 is patentable.

Amended claim 48 sets forth integrated circuitry that includes, among other features, a layer of electrically insulating material over a semiconductive substrate, a series of alternating first and second conductive lines directly over the layer of insulating material, and intervening strips of insulating material laterally between the first and second conductive lines. The first and second conductive lines are spaced and positioned laterally adjacent one another. The first conductive lines are electrically isolated from the second conductive lines. None of the first and second conductive lines overlap any immediately laterally adjacent first or second conductive lines. As may be appreciated from the discussion above regarding some of the deficiencies of Lur as applied to claim 40, Applicant asserts that Lur in view of Choe fails to disclose or suggest every limitation of claim 48. Claims 49-

55 depend from claim 48 and are patentable at least for such reason as well as for the additional limitations of such claims not disclosed or suggested.

Applicant asserts that claims 40-55 are patentable over Lur in view of Choe and request allowance of such claims in the next Office Action.

Claims 56-58 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Chu in view of Miyanaga. Applicant requests reconsideration.

Amended claim 56 sets forth integrated circuitry that includes, among other features, a series of first conductive polysilicon lines over a BPSG layer, electrically insulative oxide material on and in contact with respective first series conductive lines and a top of the insulative oxide material over at least some of the first series conductive lines defining a first plane. The integrated circuitry includes a series of second conductive aluminum-containing lines having respective line tops at least some of which define a second plane that is coplanar with the first plane. The series of second conductive lines are electrically isolated from the first conductive lines. Pages 5-6 of the Office Action allege that Choe discloses every limitation of claim 56 except for the BPSG and aluminum-containing lines and relies upon Miyanaga as allegedly remedying such deficiencies. Applicant asserts that Chu in view of Miyanaga fails to disclose or suggest every limitation of claim 56.

Page 5 of the Office Action states insulating layer 312 in Chu discloses the claimed electrically insulative oxide material.. Page 5 also alleges that polysilicon gates 302 disclose the claimed first conductive polysilicon lines.

However, insulating layer 312 is not on and in contact with polysilicon gates 302. Polysilicon gates 302 are isolated from insulating layer 312 by insulating layer 304 and sidewall spacers 308. Even if insulating layer 304 is considered to contact polysilicon gates 302, insulating layer 304 does not define a first plane that is coplanar with the tops of plugs 313 alleged to disclose the series of second conductive lines. At least for such reason, Chu fails to disclose every limitation of claim 56.

Also, Applicant notes that the features of Chu shown in Fig. 3O represent a memory array that is part of an integrated circuit. Accordingly, plugs 313 are not electrically isolated from polysilicon gates 302 as being parts of the same circuit. Review of Chu does not reveal any basis for expecting that such components of a memory array would nevertheless be electrically isolated. At least for such reason, Chu fails to disclose every limitation of amended claim 56.

Even though Chu is combined with Miyanaga, Applicant asserts that Miyanaga fails to remedy the deficiencies of Chu discussed above. Accordingly, claim 56 is patentable over Chu in view of Miyanaga. Claims 57 and 58 depend from claim 56 and are patentable at least for such reason as well as for the additional limitations of such claims not disclosed or suggested. Applicant requests allowance of claims 56-58 in the next Office Action.

Applicant herein establishes adequate reasons supporting patentability of claims 40-58 and requests allowance of all pending claims in the next Office Action.

Respectfully submitted,

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James E. Lake
Reg. No. 44,854